REMARKS

In the Non-Final Office Action of January 18, 2007, the Examiner (1) rejected claims 1-2, 5-7, 10-11, 14, 17, 20-21, and 23 as allegedly obvious over U.S. Patent No. 6,088,786 ("Feierbach") in view of U.S. Patent No. 6,965,984 ("Seal"), in view of U.S. Patent No. 6,549,961 ("Kloth"); (2) rejected claims 22 and 24 as allegedly obvious over "Feierbach in view of Seal, in view of Kloth further in view of U.S. Patent No. 5,951,689 ("Evoy").

Applicants believe that the pending claim are allowable over the art of record and respectfully request reconsideration.

I. ART BASED REJECTIONS

A. Claim 1

Claim 1 stands rejected as allegedly obvious over Feierbach, Seal and Kloth.

Feierbach is directed towards coupling a stack based processor to a register based functional unit. (Feierbach Title). In particular, Feierbach teaches a stack processor and register processor as part of a stack and register processor. (Feierbach Col. 6, lines 53-59). Further, Feierbach discloses a copy-unit to control access of data between the processors. (Feierbach Abstract).

Seal is directed towards data processing using multiple instruction sets. (Seal Title). In particular, in Seal the stream of Java bytecodes are provided to bytecode translation hardware 6. (Seal Col. 6, lines 10-14; Figure 1). For some bytecodes, the bytecode translation hardware 6 generates a series of ARM opcodes which are applied to the ARM opcode decoder 10. (Seal Col. 6, lines 10-29; Figure 1). For other bytecodes, (bytecodes not supported by the hardware) the bytecode translation hardware triggers a software instruction interpreter written in ARM native instructions. (Seal Col. 6, lines 30-39).

Kloth is directed towards semaphore access in a multiprocessor system. (Kloth Title). In particular, Kloth teaches an access control system for protected resources. (Kloth Abstract). In Kloth, a processor requests to allocate a protected resource; this request, in turn, is forwarded to a bridge which determines whether to grant the access to the protected resource. (Kloth col. 3, lines 51-67 to col. 4, lines 1-2). The bridge determines if the requested resource is available, and if it is available the request is granted to processor. (Kloth Col. 3, lines 61-66). Hence, Kloth teaches a system where if the requested resource is available then a halt signal is not asserted. Moreover,

Kloth teaches that eventually the processor granted access releases the protected resource. (Kloth Col. 4, lines 19-21). The bridge determines if there is another processor waiting to access the released resource, and if so the halt signal is deasserted on the processor. (Kloth Col. 4, lines 24-32). Further, it appears that Kloth teaches a system where if another processor is not waiting to access the resource then the halt signal is not deasserted. (Kloth Col. 4, lines 22-26).

Claim 1, by contrast, specifically recites "wherein the first processor executes a transaction targeting a pre-determined address and the synchronization unit detects said pre-determined address and asserts a wait signal to cause said first processor to enter a reduced power or reduced performance mode; and wherein said second processor asserts a wait release signal that is received by said synchronization unit and that causes said synchronization unit to deassert said wait signal to the first processor." Applicants submit that Feierbach, Seal and Kloth fail to teach or fairly suggest such a system. First, Kloth teaches a system in which; if the requested resource is available the system does not assert a halt signal. Thus, even if hypothetically the teachings of Feierbach and Seal are precisely as the Office action suggests (which Applicants do not admit), Feierbach, Seal and Kloth still fail to teach or suggest "wherein the first processor executes a transaction targeting a pre-determined address and **the synchronization unit detects said pre-determined address and asserts a wait signal to cause said first processor to enter a reduced a power or reduced performance mode**." Second, Kloth also appears to teach a system in which if another processor is not waiting to access the released resource then the halt signal is not deasserted. Thus, even if hypothetically the teachings of Feierbach and Seal are precisely as the Office action suggests (which Applicants do not admit), Feierbach, Seal and Kloth still fail to teach or suggest "wherein said second processor asserts a wait release signal that is received by said synchronization unit and that causes said **synchronization unit to deassert said wait signal to the first processor**."

Based on the foregoing, Applicants respectfully submit that claim 1, and all claims which depend on claim 1 (2, 5-7, and 20-22), should be allowed.

B. Claim 10

Claim 10 stands rejected as allegedly obvious in over Feierbach, Seal and Kloth

Claim 10 specifically recites "wherein synchronizing comprises detecting that the first processor is executing a transaction targeting a pre-determined address and asserting a wait signal to cause said first processor to enter a reduced power or reduced performance mode and

synchronizing further comprises the second processor causing the wait signal to be de-asserted to terminate the first processor's reduced power or reduced performance mode." Applicants submit that Feierbach, Seal and Kloth fail to teach or fairly suggest such a system. First, Kloth teaches a system in which; if the requested resource is available the system does not assert a halt signal. Thus, even if hypothetically the teachings of Feierbach and Seal are precisely as the Office action suggests (which Applicants do not admit), Feierbach, Seal and Kloth still fail to teach or fairly suggest "wherein synchronizing comprises **detecting that the first processor is executing a transaction targeting a pre-determined address and asserting a wait signal to cause said first processor to enter a reduced power or reduced performance mode**." Second, Kloth also appears to teach a system in which if another processor is not waiting to access the released resource then the halt signal is not deasserted. Thus, even if hypothetically the teachings of Feierbach and Seal are precisely as the Office action suggests (which Applicants do not admit), Feierbach, Seal and Kloth still fail to teach or fairly suggest "synchronizing further comprises the second processor causing **the wait signal to be de-asserted to terminate the first processor's reduced power or reduced performance mode**."

Based on the foregoing, Applicants respectfully submit that claim 10, and all claims which depend on claim 10 (11, 14), should be allowed.

C. Claim 17

Claim 17 stands rejected as allegedly obvious in over Feierbach, Seal and Kloth.

Claim 17 specifically recites "a synchronization unit coupled to the first and second processors, said synchronization unit asserts a first signal to the first processor to cause the first processor to cease executing instructions and said synchronization unit receives a second signal from second processor which thereby causes the synchronization unit to de-assert the first signal." Applicants submit that Feierbach, Seal and Kloth fail to teach or fairly suggest such a system. First, Kloth teaches a system in which; if the requested resource is available the system does not assert a halt signal. Thus, even if hypothetically the teachings of Feierbach and Seal are precisely as the Office action suggests (which Applicants do not admit), Feierbach, Seal and Kloth still fail to teach or fairly suggest "a synchronization unit coupled to the first and second processors, said **synchronization unit asserts a first signal to the first processor to cause the first processor to cease executing instructions**." Second, Kloth also appears to teach a system in which if another

processor is not waiting to access the released resource then the halt signal is not deasserted. Thus, even if hypothetically the teachings of Feierbach and Seal are precisely as the Office action suggests (which Applicants do not admit), Feierbach, Seal and Kloth still fail to teach or fairly suggest "synchronization unit receives a second signal from second processor which thereby **causes the synchronization unit to de-assert the first signal**."

Based on the foregoing, Applicant respectfully submit that claim 17, and all claims which depend on claim 17 (23, 24), should be allowed.

II. CONCLUSION

In course of the foregoing discussions, Applicants may have at times referred to claim limitations in shorthand fashion, or may have focused on a particular claim element. This discussion should not be interpreted to mean that the other limitations can be ignored or dismissed. The claims must be viewed as a whole, and each limitation of the claims must be considered when determining the patentability of the claims. Moreover, it should be understood that there may be other distinctions between the claims and cited art which have yet to be raised, but which may be raised in the future.

Applicants respectfully request reconsideration and that a timely Notice of Allowance be issued in this case. If the Examiner feels that a telephone conference would expedite the resolution of this case, he is respectfully requested to contact the undersigned. It is believed that no extensions of time or fees are required, beyond those that may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required (including fees for net addition of claims) are hereby authorized to be charged to the Texas Instruments, Inc. Deposit Account No. 20-0668.

Respectfully submitted,

/Utpal D. Shah/

Utpal D. Shah
PTO Reg. No. 60,047
CONLEY ROSE, P.C.
(512) 391-1900 (Phone)
(512) 320-9182 (Fax)
AGENT FOR APPLICANTS